

Advanced Traffic Management and Congestion Control Capabilities in ATM Architecture

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Abstract—To meet the demands of multiservice networking, in which traffic of varying bandwidth and delay requirements must be simultaneously serviced, sophisticated traffic and resource management mechanisms are needed. To serve these needs, your ATM switch router uses a shared-memory architecture that offers advanced traffic management and congestion control capabilities. The traffic management features of the ATM switch router provide the following capabilities:

- Integrated support for different types of ATM services
- Flexible policies for bandwidth allocation through controlled link-sharing services.
- Effective use of network resources
- The congestion control capabilities of the ATM switch router support the following goals:

Avoid conditions where congestion can occur.

- Minimize the effects of congestion when it does occur.
- Prevent spreading the congestion state to other parts of the network.

The specific resource management capabilities of your ATM switch router are platform dependent.

I. LITERATURE SURVEY

This proposal from France Telecom requires sources to send a resource management RM cell requesting the desired bandwidth before actually sending the cells. If a switch cannot grant the request it simply drops the RM cell the source times out and resends the request if a switch can satisfy the request it passes the RM cell on to the next switch. Finally the destination returns the cell back to the source, which can then transmit the burst. As described above, the burst has to wait for at least one round trip delay at the source even if the network is idle as is often the case. To avoid this delay, an immediate transmission IT mode was also proposed in which the burst is transmitted immediately following the RM cell, If a switch cannot satisfy the request it drops the cell and the burst and sends

an indication to the source, If cell loss rather than bandwidth is of concern the resource request could contain the burst size A switch would accept the request only if it had that many buyers available.

The fast resource management proposal was not accepted at the ATM Forum primarily because it would either cause excessive delay during normal operation or excessive loss during congestion.

II. INTRODUCTION

Available Bit Rate mechanisms allow the network to allocate the available bandwidth fairly and efficiently among the ABR sources (fig. 1). ABR sources limit their data transmission to rates allowed by the network.

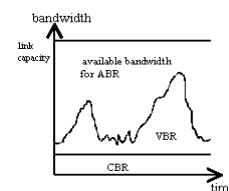


Fig. 1. Available ABR bandwidth

The network consists of switches, which use locally available information to calculate the explicit, allowable rates or relative rate indications (e.g. to decrease rate) for the source. This feedback information is sent to the sources using Resource Management cells (RM-cells). RM-cells are generated by the source and travel along the data path to the destination. After toggling the direction bit of the RM-cells, the destination returns the RM-cells to the source. The switches might modify the passing RM-cells.

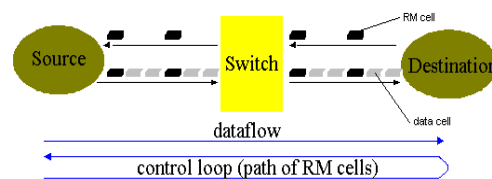


Fig. 2. ABR Control Loop

For very large networks or networks using satellite links, the round trip delay of the RM-cells potentially cause instabilities. Therefore, ATM Forum’s Traffic Management Specifications describe a partitioning of the network into smaller loops by using several virtual sources/destinations (VS/VD) implemented in the switches. VS/VD implementation exceeds the scope of this introduction and is therefore not further treated here.

The software requirements analysis (SRA) step of a software development process yields specifications that are used in software engineering. If the software is “semiautomatic” or user centered, software design may involve user experiences design yielding a story board to help determine those specifications. If the software is completely automated (meaning no user or user interface), a software design may be as a flowchart or text describing a planned sequence of events. In either case some documentation of the plan is usually the product of the design.

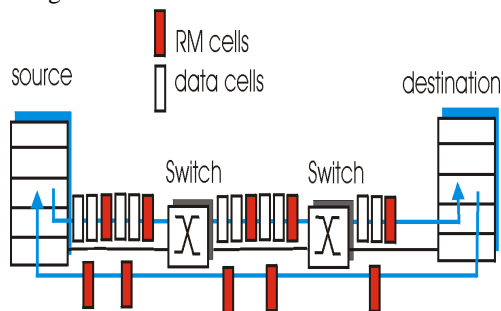


Fig. 3. ABR Control Loop

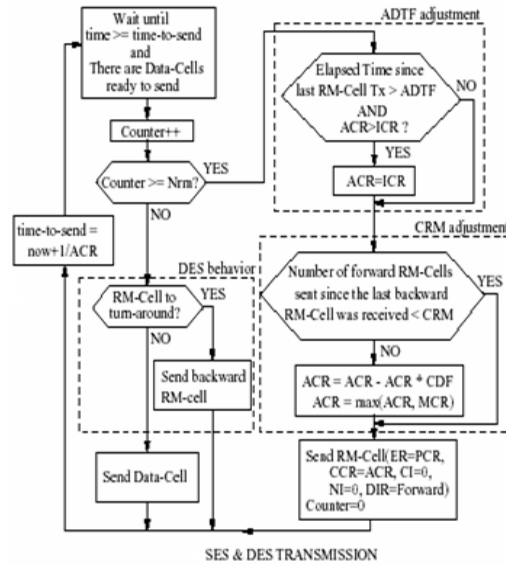
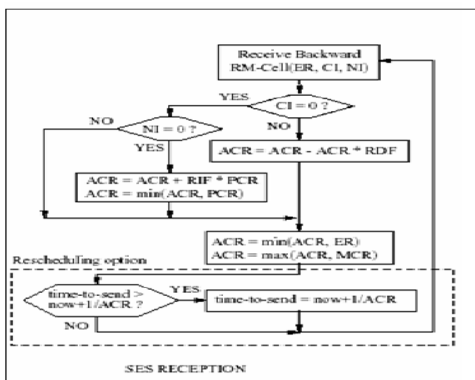


Fig. 4. SES & DES Transmission

Every computer on an IP network is identified by a 4-byte number. This is normally written in a format like 199.1.32.90, where each of the four numbers is one unsigned byte ranging in value from 0 to 255. Every computer attached to an IP network has a unique 4-byte address. When data is transmitted across the network in packets, each packet's header includes the address of the machine for which the packet is intended (the destination address) and the address of the machine that sent the packet (the source address). Routers along the way choose the best route to send the packet along by inspecting the destination address. The source address is included so that the recipient will know who to reply to.

Each computer with an IP address has several thousand logical ports (65,535 per transport layer protocol, to be precise). These are purely abstractions in the computer's memory and do not represent anything physical like a serial or parallel port. Each port is identified by a number from 1 to 65,535. Each port can be allocated to a particular service.

III. RESULTS

There are many approaches to software testing, but affective testing of complex products is essentially a process of investigation, not merely a matter of creating and following routine procedure. One definition of testing is “the process of questioning a product in order to evaluate it”, where the “questions” are operations the tester attempts to execute with a product, and the product answers with its behavior in reaction to the probing of the tester. Although most of the intellectual process of testing is nearly identical to that of

review or inspection, the word testing is connoted to mean the dynamic analysis of the product putting the product through its paces. Some of the common quality includes capability, reliability, efficiency, portability, maintainability, compatibility and usability. A good test is some times describe as one which reveals an error however, more recent thinking suggest that a good test is one which reveals information of interest to some one who matters within the project community.

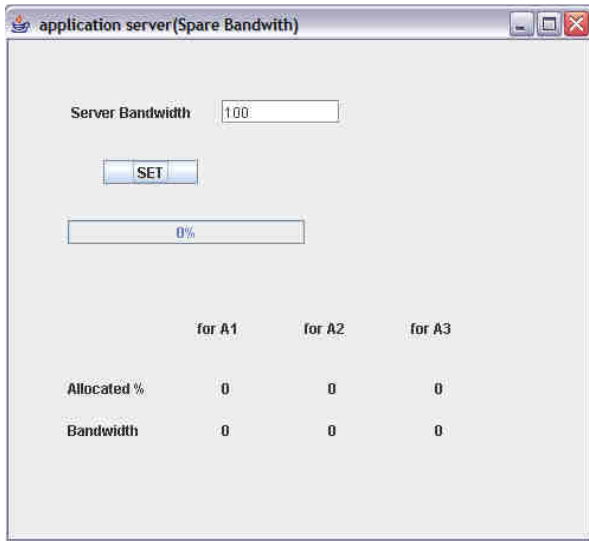


Fig. 5. Spare Bandwidth Application Server

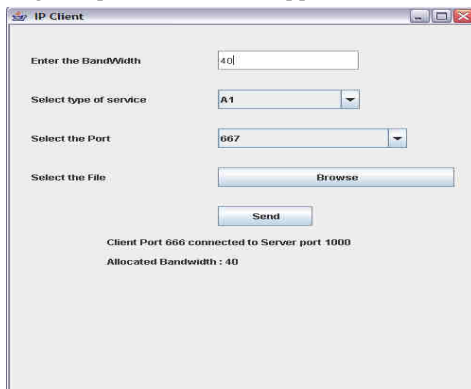


Fig. 6. IPclient

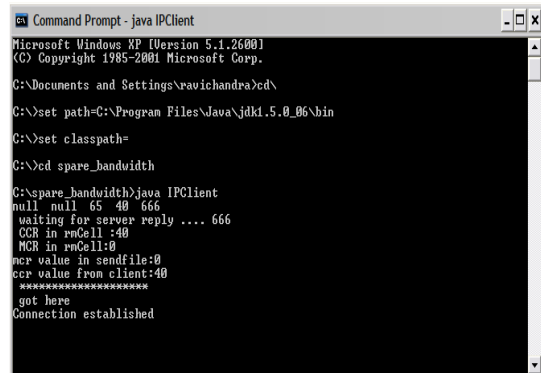


Fig. 7. IPclient

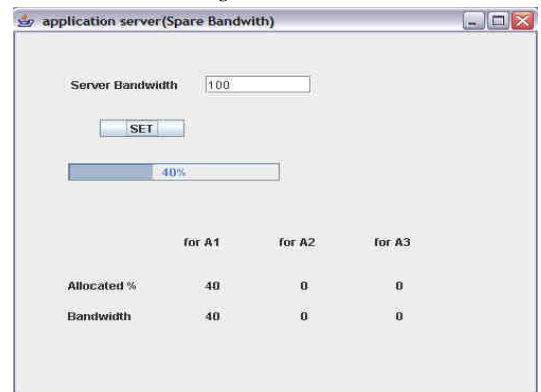


Fig. 8. Spare Bandwidth (100)

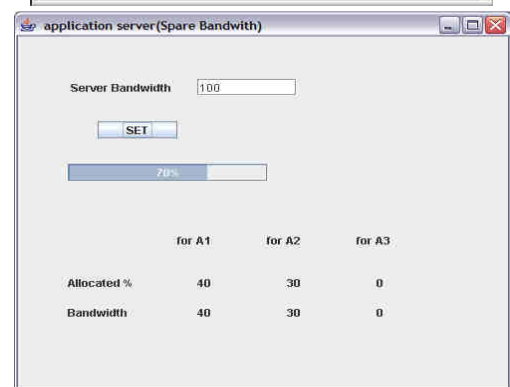
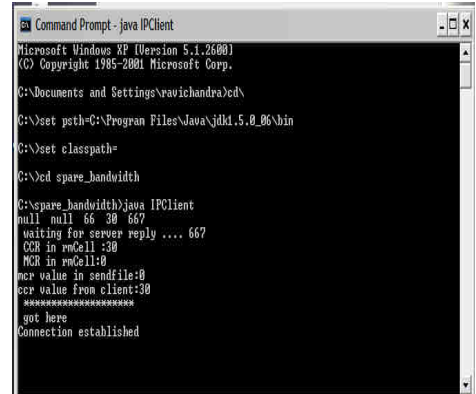


Fig. 9. Allocated and Spare Bandwidth

