# Implementation of High Speed MAC VLSI Architectures, Based on High Radix Modified Booth Algorithm

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***Abstract****—Now a day the multimedia communication and digital signal processing systems are increasing which demand for high speed, low power consumption and lower delay. Addition as well as Multiplication is one of the key features of such systems. It is thought to propose a new architecture of multiplication and accumulation unit for parallel processing for addition and multiplication. The proposed architecture uses modified booth algorithm, Wallace tree and carry save adder. Modified Booth algorithm is suggested to reduce the partial products and CSA is utilized for improving the design speed. The proposed design is developed, simulated and synthesized using Xilinx ISE showing the results in terms of reduced delay and lower power.*

***Keywords— Booth multiplier, MAC, High-speed, Radix, VLSI, Xilinx ISE, FPGA.***

## I. INTRODUCTION

Different multiplier architectures have been proposed amid the previous couple of decades. The multiplier is one of the key equipment hinders in the greater part of the advanced and superior frameworks, for example, computerized signal processors and microchips. With the late advances in innovation, numerous specialists have taken a shot at the outline of progressively more effective multipliers. They go for offering higher speed and lower force utilization even while occupying decreased silicon region. This makes them good for different intricate and versatile VLSI circuit usage. In any case, the reality remains that the speed and operating frequency are two crucial performance imperatives. Subsequently, advancing expanded speed dependably brings about more area utilization. A few multiplication algorithms are utilized to accomplish multiplications which are based on parallel and serial multiplication. Parallel multiplication is constantly invaluable over sequential. Commonly, binary multiplication is possible by using Vedic multiplier [1]. On the other hand, it is not suitable for 2's supplements numbers. In this way, to accomplish parallel duplication, Baugh-Wooly's 2's complement multiplication calculation is generally utilized [1, 2]. Booth's algorithm is likewise utilized much of the time for 2's supplement numbers. Booth's calculation utilizes radix recoding to accomplish high speed [3]. Increment in radix produces diminished number of partial products. Higher radix recoding has noteworthy utilization in rapid computerized arithmetic. The fundamental multipliers in light of corner calculation are successive multipliers. Then again, Booth's exhibit duplication is another system to accomplish multiplication. These sorts of array multipliers comprise of a fundamental unit of addition, subtraction and shifting. It likewise requires little controller to control all the operation in the multiplier relying upon information vectors.

The key challenges of the Multiplier are:

**Speed:** In recent years multimedia communication and signal processing are increasing rapidly due to this growth data processing is also increasing. These applications are performed by repetitive use of multiplication and addition (which is performed by multiplication and accumulation (MAC)). At this stage speed of multiplication and addition becomes the key parameter for performance of the system. So, there is a need to enhance the speed of multiplication and addition, in order to decrease the delay in multimedia communication.

**Power:** Due to the lower speed of the addiction and multiplication, transmission or processing time increases which causes the more power consumption to perform the operation. Due to the excessive power consumption it becomes the challenging task.

**Area:** As the multimedia communication is increasing, the portability of multimedia devices is also increasing. For this portability issue area is the main parameter. Area of the device depends on the placement of gates on the chip. If gates are placed irregularly, it utilizes more area and if gates are placed in regular way it utilizes lesser area.

**Motivation:** The existing approaches suffer from the above mentioned issues. Hence these issues become major component in the field of multimedia or signal processing systems. Speed, power and area depend on the design of the circuitry. So a new approach is required to perform low power area efficient fast architecture for these applications. For multiplication Booth algorithm is used mostly.

**Contribution:** In this work a new architecture of booth's algorithm for multiplication is proposed which reduces the area utilization, increases the speed and reduces the power consumption of the booth multiplier.

**Organization:** This paper is organized into the following sections: Section II gives the related work, Section III Explains the background and Section IV gives the problem definition, Section V explains the system Model, Section VI describes the algorithms, the performance evaluation of the proposed system model is given in Section VII, and Conclusions are given in Section VIII.

## II. RELATED WORK

In this section brief discussion is presented about the recent approaches for booth multiplication algorithms. Multiplication and accumulation are the key blocks of high performance system like filters, digital signal processors etc. In these systems speed is the key component for performance analysis. To improve the system performance new multiplier architecture of multiplier by using Modified Radix-4 booth algorithm with Binary Adder which is based on redundancy is proposed in [4]. Haimin Chen,et al.[5] proposed new procedure for the transfer of negative PP taking into account Radix-4 Booth calculation. Through recombining PP, it propels an advanced technique evading the added substance arithmetic of "in addition to 1" when figuring the supplement for negative PP, without expanding new PP. The trial result demonstrates to it could clearly enhance the execution of multiplier. This technique is of incredible essentialness for shortening the key way of multiplier and after that enhancing its execution speed, which could be connected in all multipliers taking into account Radix-4 Booth encoding. One of the powerful approaches to accelerate multiplication is by diminishing the quantity of fractional products and quickening the aggregation. Another construction modeling of half breed Modified Booth Encoded Algorithm (MBE) and Carry Save Adder (CSA) is proposed as quick multiplier structural planning [6]. S.Saravanan et al. [7] proposed a setup of a low power consumption Hybrid Encoded Booth Multiplier (HEBM) with Reduced Switching Activity Technique(RSAT). This RSAT technique has been joined on the creamer encoder of the multiplier to lessen the force usage. The cream encoder in the low power multiplier uses both the Booth and proposed strategy.

F. Elguibaly et al [8] exhibited dependence (DG) to visualize and depict combined MAC equipment that depends on the Modified Booth Algorithm (MBA). Carry save adder is utilized in this design. He apply DG MAC information word size and permits outlining multiplier structures that are normal furthermore, have negligible delay, sign-piece expansions, and information data width. He proposed a quick pipelined usage by utilizing dependence diagram, in which he utilized a precise delay model for profound submicron CMOS innovation. Suriya et al. [9] proposed a new architecture of MAC for fast arithmetic operations. The key part of the work is to reduce the partial product which is done by combining multiplication and accumulation. In this work they have worked on reduction of power consumption. For power reduction a new methodology spurious power suppression technique (SPST), is proposed. The work presented in [9] is efficient in terms of power but due to high speed requirement for huge data speed is the main tradeoff. To overcome this, parallel multiplier- accumulator architecture is proposed which is the combination of MAC and hybrid carry save adder. To improve the performance of modified booth algorithm multiplier and accumulator architecture is merged with the carry save adder. The proposed CSA model uses 1's complement and has the capability to perform the increment in density of bit. The proposed MAC aggregates the intermediate results in the sort of total and convey bits rather than the last adder, which made it conceivable to enhance the pipeline plan to enhance the execution. Gowridevi, B.; Gangadevi et al [11] proposed a new framework Modified Booth Multiprecision Multiplier (MBMP) for reducing the power. In this model small precision multiplier are selected based on the input operands. This work proposes the architecture to reduce the area overhead also. In this design the numbers of partial products are reduced form N to N/2 by using modified booth algorithm. In the same way for reducing the area Jintao Jiang et al [12] proposed new method for optimization of layout of the design. In this work they used complementary pass-transistor adiabatic logic to achieve the energy efficient design. This work is done by using modified booth algorithm and results were carried out by using TSMC 0.18μm CMOS process technology with full-custom layouts and parasitic extraction.

## III. PROPOSED MODEL

These section focuses on the design approach for Booth multipliers by considering the necessary specifications for develop the relevant source code in VHDL.

In this work our main aim to propose a new design for parallel multiplication-accumulation based on the modified booth algorithm. In order to design the architecture first

stage to design the multiplication-accumulator architecture, then designing the Wallace tree multiplier, next step is to design carry save adder (CSA), and finally MAC and CSA are merged to evaluate the performance of the proposed system architecture.

The proposed multiplier architecture consist three parts: Booth encoder model, Wallace tree for compressing the partial products, final adder. Since the proposed model is based on the parallel multiplication so to add the partial products in parallel manner we use Wallace tree structure. In section II we have seen that the speed can be increased by minimizing the partial products. To reduce the number of partial product, modified booth algorithm is used and with the help of Wallace tree speed is optimized of the proposed architecture.

## MULTIPLICATION-ACCUMULATION ARCHITECTURE

Define In this section we discuss about the multiplication and accumulation architecture. MAC is mainly used for multimedia or digital signal processing equipment for fast processing of data. This is used to solve the expression as:

$$y[n] = \sum_{k} x[k]h[n-k] \qquad \text{Eq. (1)}$$

According to the equation (1), first of all multiplication is performed for all the values of x and h, finally addition operation is performed to get the output. Rather than waiting for the multiplication results, addition operation is performed parallel with the help of MAC model.

The common expression of MAC is given below:

$$y[n+1] = y[n] + x[n+1] * h[n+1] \qquad \text{Eq. (2)}$$

In the above equation (2) $x$ represents the multiplier and multiplicand for $n$ bit is given by

The multiplier can be divided into three parts: (i) Generation of partial product (ii) Compression of partial products and (iii) Addition

Partial products are generated by using multiplicand and multiplier. In this next stage compression of partial product is performed and finally addition is performed in adder block. In the figure 1 multiplier and accumulator hardware architecture is shown.

The multiplicand and multiplier need to represent in 2's complement which is given by

$$Multiplicand = -2^{\mathcal{N}-1}x_{\mathcal{N}-1} + \sum_{i=0}^{\mathcal{N}-2} x_i 2^i, \qquad x_i \epsilon\, 0,1 \qquad \text{Eq. (3)}$$

Where $\mathcal{N}$ is the total number of bits.

Equation (3) gives the redundant sign bits in the base -4 format, to apply the Booth algorithm; it can be converted by using equation (4)

$$Multiplicand = \sum_{i=0}^{\mathcal{N}/2-1} \delta_i 4_i, \qquad \text{Eq. (4)}$$

$\delta_i$ is given by

$$Multiplicand = -2x_{2_{i+1}} + x_{2i+1} + x_{2i-1} \qquad \text{Eq. (5)}$$

Now, the multiplication of multiplicand d and multiplier can be expressed as

$$Multiplicand \times Multiplier = \sum_{i=0}^{\mathcal{N}/2-1} d_i 2^{2i} \times Multiplier \qquad \text{Eq. (6)}$$

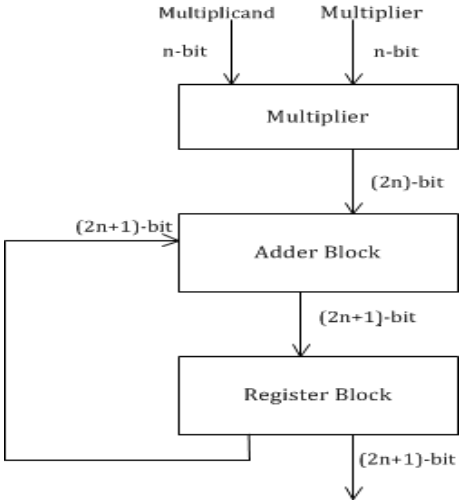


*Fig.1: MAC Architecture*

By using these equation the multiplication and accumulation can be given as

$$Out = Multiplicand \times Multiplier + (2n+1)bit\ of\ adder\ block\ from\ register \qquad \text{Eq. (7)}$$

In other way it can be defined as

$$Out = \sum_{i=0}^{\mathcal{N}/2-1} \delta_i 2^{2i} \times Multiplier + \sum_{j=0}^{2\mathcal{N}-1} Multiplcand_j 2^{2i} \qquad \text{Eq. (8)}$$

To improve the performance of the proposed MAC architecture the accumulator unit is merged with the carry save adder. In this case the critical path is computed by the final adder. The performance of final adder can be

improved by minimizing the number of input bits, in order to minimize the bits the partial products are compressed in the form of carry and sum. This method is applied to the (8), to get the proposed architecture of MAC.

In order to apply this method equation (6) can be re-written as

$$Multiplicand \times Multiplier = \delta_0 2 \times Multiplicand + \cdots + \delta_{\frac{\mathcal{N}}{2}-1} 2^{\mathcal{N}-2} \times Multiplicand \quad \text{Eq. (9)}$$

The partial products from the above equation can be given as

$$Multiplicand \times Multiplier = \delta_0 2 \times Multiplicand + \sum_{i=1}^{\frac{\mathcal{N}}{2}-2} \delta_i 2^{2i} \times Multiplicand + \delta_{\frac{\mathcal{N}}{2}-1} 2^{\mathcal{N}-2} \times Multiplicand \quad \text{Eq.(10)}$$

In figure 2 the proposed multiplication and accumulation architecture is given. To differentiate the sum, carry and added results partial products are divided. The same method is applied for the equation (7) (2n+1) bits.

By analyzing and rearranging equation (7) it can be expressed as

$$z = \sum_{i=0}^{\mathcal{N}-1} z_i 2^{2i} + \sum_{i=\mathcal{N}}^{2\mathcal{N}-1} z_j 2^{2i} \quad \text{Eq. (11)}$$

$z$ is the representation of number of bits at the adder stage in equation (7). The value of sum and carry (which is called first stage) is computed by using equation (11), the computation of second stage is done by using equation (12). It can be divided into sum and carry.

$$\sum_{i=\mathcal{N}}^{2\mathcal{N}-1} z_j 2^{2i} = \sum_{i=0}^{\mathcal{N}-1} z_{\mathcal{N}+1} 2^{2i} 2^{\mathcal{N}} = \sum_{i=0}^{\mathcal{N}-2} (Carry_i + Sum_i) 2^{2i} 2^{\mathcal{N}} \quad \text{Eq. (12)}$$

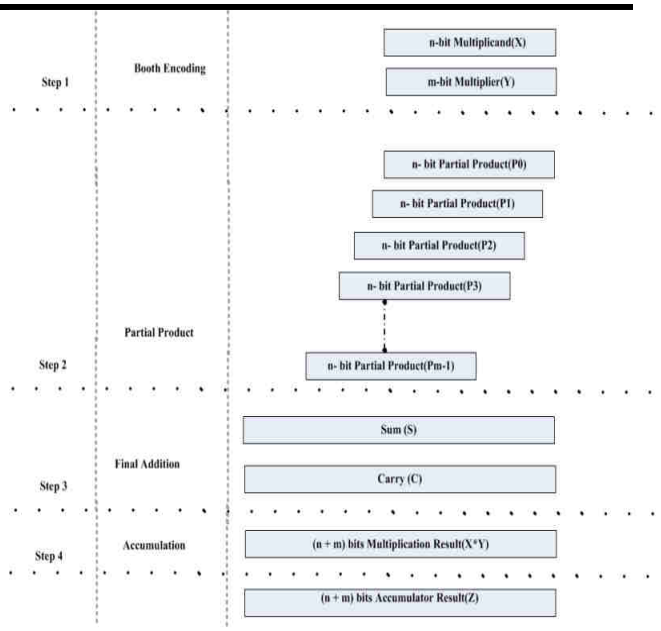


*Fig.2: Proposed arithmetic operation of multiplication and accumulation*

Finally, separated steps can be written as

$$Z = \sum_{i=0}^{\mathcal{N}-1} z_i 2^{2i} + \sum_{i=0}^{\mathcal{N}-2} Carry_i 2^{2i} 2^{\mathcal{N}} + \sum_{i=0}^{\mathcal{N}-2} Sum_i 2^{2i} 2^{\mathcal{N}} \quad \text{Eq. (13)}$$

With the help of equation (6) and (11), final MAC can be written as

$$Out = (\delta_0 2 \times Multiplicand + \sum_{i=0}^{\mathcal{N}-1} z_i 2^{2i}) + \left( \sum_{i=1}^{\mathcal{N}-2} d_i 2^{2i}\, Multiplicand + \sum_{i=0}^{\mathcal{N}-2} carry_i 2^{2i} 2^{\mathcal{N}} \right) + \left( \delta_{\frac{\mathcal{N}}{2}-1} 2^{\mathcal{N}-2} MCand + \sum_{i=0}^{\mathcal{N}-2} sum_i 2^i 2^{\mathcal{N}} \right) \quad \text{Eq. (14)}$$

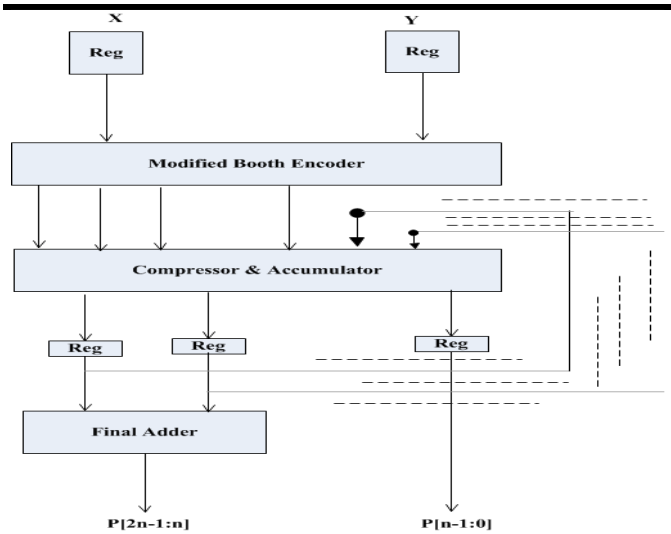


*Fig.3: Proposed MAC Architecture*

The above given figure 3 shows the hardware architecture of the proposed multiplication and accumulation model.

## IV. WALLACE TREE

Wallace multiplier consist three main steps: (i) multiply each bit with another input's each bit achieving N^2 results. Based on the position of multiplicand and their weights reduce the partial products. In second stage in the event that there are three or more wires with the same weight and a taking after layer: Take any three wires with the same weights and information them into a full adder. On the off chance that there are two wires of the same weight left, enter them into a half adder. If there are two wires of the same weight left, enter them into a half adder. On the off chance that there are two wires of the same weight left, enter them into a half adder. In the event that there is only one wire left join it to the following layer. The benefits of utilizing the Wallace tree construction modeling is, every one of the bits of all of halfway items in every segment are included in parallel free of different sections. In the ordinary 8 bit Wallace tree multiplier outline more number of expansion operations is required. Utilizing adder, three fractional item terms can be added at once to frame the convey and aggregate. A multiplier comprises of different phases of fulladders, each higher stage means the aggregate deferral of the framework. In the first and second phases of the Wallace structure, the fractional items don't rely on some other qualities other than the inputs acquired from the AND cluster. However for the prompt higher stages, the last esteem (PP3) relies on upon the Cout estimation of past stage. This operation is rehashed for further stages. Consequently, the significant reason for deferral is the complete's spread from the aggregate number of stages in the basic way.

### Modified Booth Algorithm

In this section we discuss about the modified booth algorithm. In the literature survey we have studied that modified booth algorithm is more efficient in terms of area, delay and power. In our proposed model we use modified booth algorithm for simulation analysis. It is a redundant signed digit radix-4 method. It reduces the number of partial product compare to other existing radix-2 or radix-4 algorithm. The Modified Booth Multiplier was proposed by O. L. Macsorley in 1961. It is used for generating partial products for large multipliers.

Let us consider X is a multiplicand and Y is a multiplier which are in the form of 2's complement representation. The multiplicand Y can be given according to Modified Booth algorithm as:

$$Y = (y_{n-1}y_{n-2} \dots y_1y_0)$$

$$= -y_{2\mathcal{N}-1}.2^{2\mathcal{N}-1} + \sum_{i=0}^{2\mathcal{N}-2} y_i.2^i \quad \text{Eq. (15)}$$

$$(y_{\mathcal{N}-1}{}^{MB}y_{\mathcal{N}-2}{}^{MB} \dots y_1{}^{MB}y_0{}^{MB}) = \sum_{j=0}^{\mathcal{N}-2} y^{MB}{}_i.2^{2j} \quad \text{Eq. (16)}$$

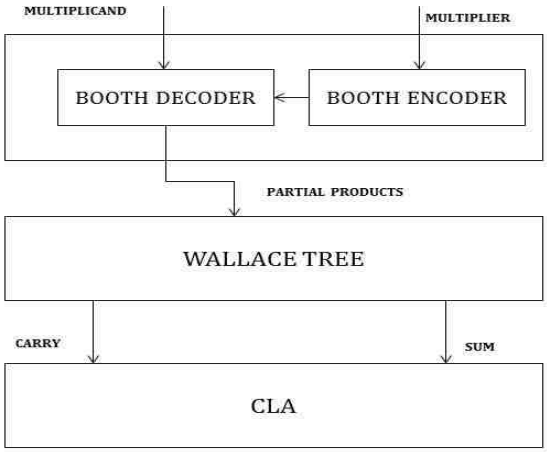


*Fig.4: Modified Booth Algorithm Architecture*

Booth multiplication is a strategy that considers littler, speedier duplication circuits, by recoding the numbers that are increased [12]. It is conceivable to diminish the quantity of fractional items considerably, by the procedure of radix-4 Booth recoding. The fundamental thought is that, rather than moving and including for each section of the multiplier term and increasing by 1 or 0, we just take each second segment, and duplicate by ±1, ±2, or 0, to get the same results. To Booth recode the multiplier term, we consider the bits in squares of three, such that every piece covers the past piece by one piece. Gathering begins from the LSB, and the first piece just uses two bits of the multiplier.

*Table.1: Booth Encoding*

| Block | Coded Digit | X Operation |
|---|---|---|
| 000 | 0 | 0X |
| 001 | +1 | +1X |
| 010 | +1 | +1X |
| 011 | +2 | +2X |
| 100 | -2 | -2X |
| 101 | -1 | -1X |
| 110 | -1 | -1X |
| 111 | 0 | 0X |

The multiplier's encoding Y, utilizing the changed corner calculation, produces the accompanying five marked digits, - 2, - 1, 0, +1, +2. Each encoded digit in the multiplier performs a sure operation on the multiplicand, X, as represented in Table.1.

## V. RESULTS

Finally In this section we discuss about the results obtained for the proposed design. In table 2 synthesis results are presented for the Wallace tree multiplier. In this table slice LUTs, LUT-FF pairs and IOBs are presented.

**Synthesis Results for the Wallace Tree Multiplier**

*Table.2: Synthesis results for Wallace tree*

| Logic Utilization | Used | Available |
|---|---|---|
| Slice LUTs | 359 | 63400 |
| LUT FF pairs | 0 | 359 |
| Bonded IOBs | 210 | 320 |

**Synthesis Results for Carry save adder**

*Table.3: Synthesis results for Carry save adder*

| Logic Utilization | Used | Available |
|---|---|---|
| Slice LUTs | 58 | 63400 |
| LUT FF pairs | 0 | 359 |
| Bonded IOBs | 98 | 320 |
| Delay | 8.795 ns | |

Below given table 4 presents the cumulative results for the overall proposed architecture

*Table.4: Overall architecture synthesis result*

| Logic Utilization | Used | Available |
|---|---|---|
| 4 input Slice LUTs | 878 | 1536 |
| Occupied Slices | 473 | 768 |
| Bonded IOBs | 64 | 320 |
| Delay | 12.728ns | |

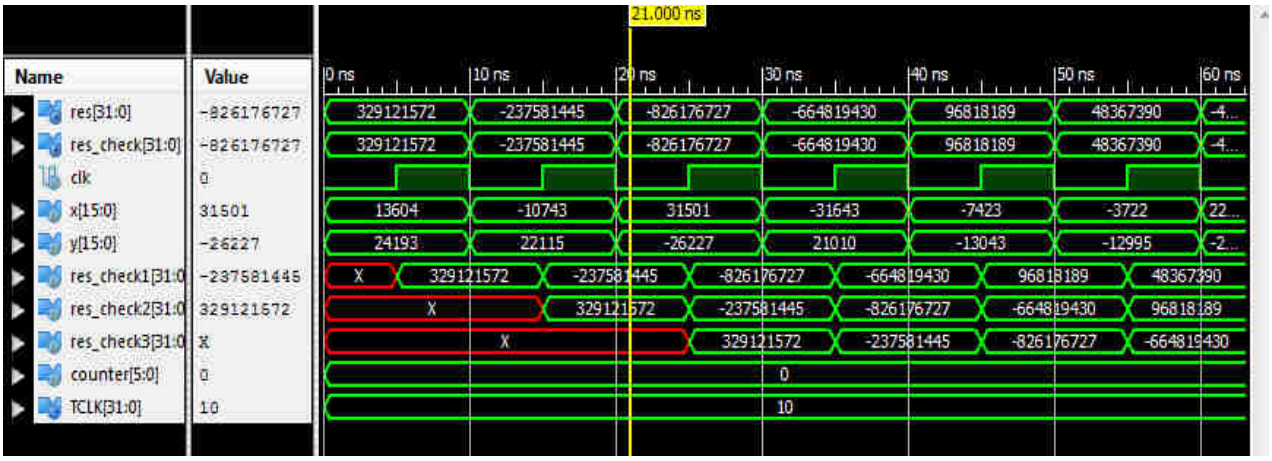


*Fig.5: Simulation waveform*

In the above given figure simulation waveform is shown. Initial inputs are x=31501 and y = -26227 which produces the multiplication result as -826176727 which is verified manually and with simulation.

For verification of the results in 2nd case we consider x= 31501 and y = 26227 which gives the multiplication results as -826176727, shown in the below given figure.

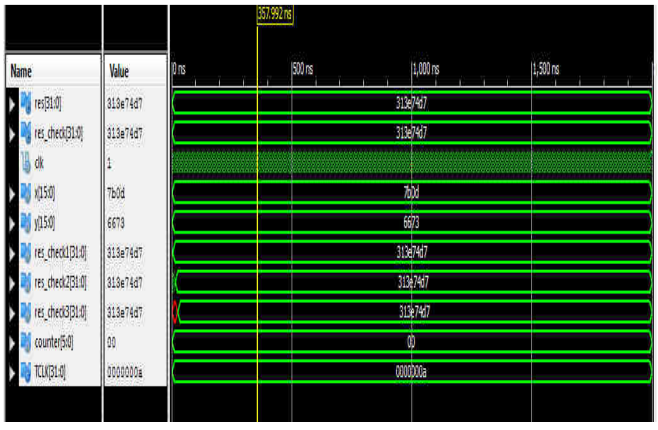

*Fig .6: Multiplication result for case 2*

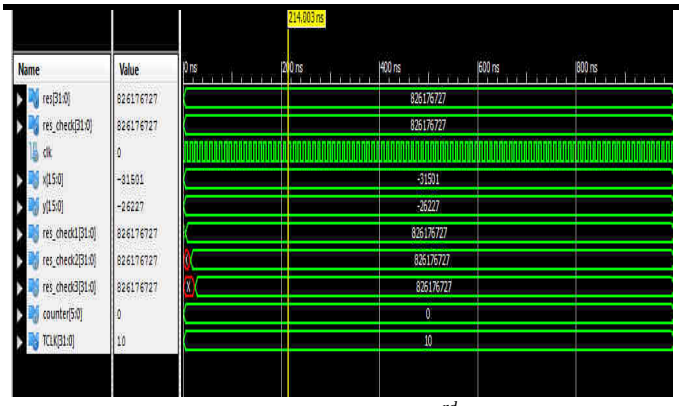


*Fig.7: Simulation result for 3rd case*

Similarly we consider x=-31501 and y = -26227 which both are anegative inputs and output is given as 826176727.

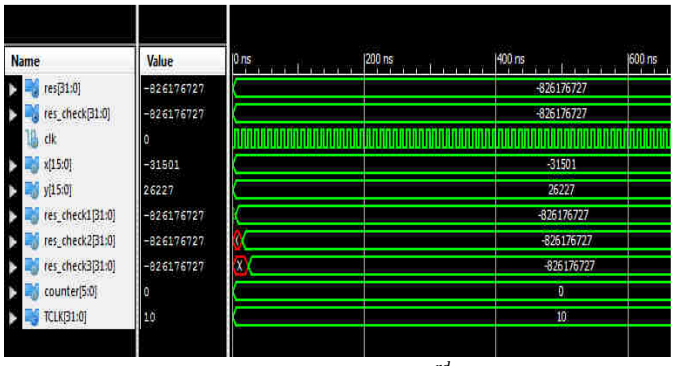


*Fig.8: Simulation result for 3rd case*

Similarly we consider x=-31501 and y =+26227 which both are negative inputs and output is given as -826176727.

Power consumption results are computed by using xPower analyzer tool.

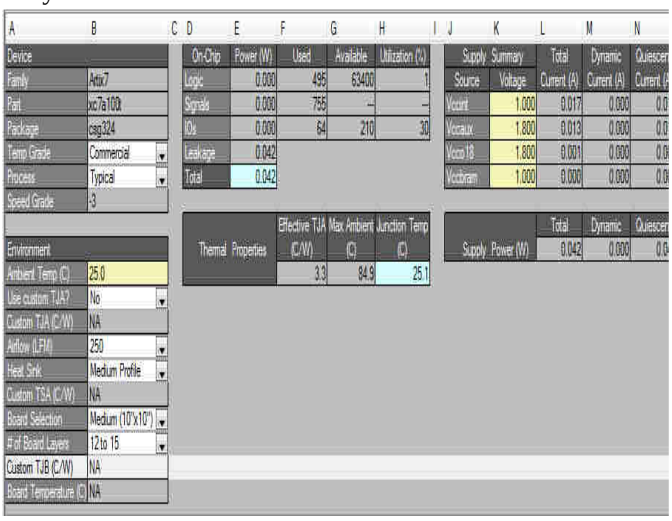


*Fig.9: Power Results By using xPower Tool*

*Table.5: Power Results generated by Xilinx ISE*

| Power Supply Currents | | | |
|---|---|---|---|
| Supply Source | Supply voltage | Total Current(mA) | Quiescent Current (mA) |
| Vccint | 1 | 16.58 | 16.58 |
| Vccaux | 1.8 | 13.14 | 13.14 |
| Vcc018 | 1.8 | 1.00 | 1.00 |
| Vccbram | 1 | 0.35 | 0.35 |

*Table.6:. Comparison of frequency and delay of various multiplier architectures*

| Algorithm used | Frequency (MHz) | Time (ns) |
|---|---|---|
| Booth algorithm | 32.84 | 30.448 |
| Modified Booth algorithm | 45.982 | 21.747 |
| Urdhwa-Tiryakbhyam | 61.869 | 16.163 |
| Compressor based Urdhwa Tiryakbhyam | 69.153 | 14.41 |
| Proposed Method | 78.61 | 12.72 |

## VI. CONCLUSION

In this paper, a new architecture of multiplier – accumulator is proposed, which is a key parameter in multimedia communication. The proposed models consist of modified Booth algorithm, Wallace tree and carry save adder. The novelty of proposed system lies in the reduction of the partial products by using the modified Booth algorithm for parallel processing. The proposed design shows the better results in fig 5,6,7,8 and in table 5 ,6 in terms of power consumption, area and delay which are the key component of any circuit.

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