Implementation of Input Oriented Dynamic Voltage and Frequency Scaling for Multiplier on FPGA

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Abstract—*This paper presents an Implementation of Dynamic voltage and frequency scaling according to input data. In the conventional method the power supply is fixed and independent on workload, so, voltage and area will be consumed unnecessary .Paper proposes the approach which focuses on making system dynamic for low power digital multiplier on reconfigurable device FPGA (Spartan III). For making system Dynamic input workload should be known and scanning is used to detect range of input so system can adjust voltage and frequency. Control signal generated from scanning which can dynamically change voltage and frequency for low power consumption according to input data.*

Keywords—Input oriented, low power, reconfigurable device, scaling, scanning.

I. INTRODUCTION

The high computation speed, low cost, and at low voltage operated systems, with low efficient use of silicon area is need of Electronics world. All the analog signal processing systems are replaced with Digital signal processing systems. DSP can perform extensive operations, and the digital multipliers are essential arithmetic block in digital signal processors. Multipliers are not used in multiplications it can be used in variety of operations such DSP applications: convolution, filtering 3Dgraphics, vector quantization. For embedded applications, it has become essential to design more power –aware multipliers. Due to varying nature of application the workload requirement is varying and below the maximum word length. One of the more effective and widely used is scanning the input data for power aware computing [1]. Digital multiplier is implemented in reconfigurable device as FPGA. As we know FPGA have number of LUT's, Transistors, Registers, IO's, for effectively use of these resources, adaptive system development is necessary. An increasingly important figure-of-merit of a VLSI system is "power awareness," which is its ability to scale power consumption in response to changing operating conditions. These changes might be brought about by the time-varying nature of inputs, desired output quality, or just environmental conditions [2]. The main advantage of Energy aware design is they can do large number of operations with different operating conditions. This is in contrast to traditional low power design for the worst case scenario, which may not be globally energy efficient. The main focus of Energy-aware designs is enabling architectures which scale down energy as quality requirements are relaxed [3].

The analog signal processing circuits are replaced with digital signal processing for their increased capabilities. The amount of power dissipation is usually limitation of degree of complexity of signal processing by which life span of battery is determining [4]. Power gating strategy is used in twin gating multiplier that automatically adapts the required precision level and disables the idle portions of the circuits to save the leakage power [5]. Power saving can be achieved by deactivating non- effective circuit area. Proposed multiplier offers tradeoff between power and output precision with varying precision levels [6].

For silicon area reduction requirement is to implement a single processing unit which taken advantage of by implementing multiple processing units operating in parallel on single silicon die. Through parallel processing, hardware for low precision fixed point can be used to build in low cost [7]. A new configurable multiplier is designed which is configured with two command for signed and unsigned two complement number and it gives higher throughput at low level of precision [8].

FPGA based new arithmetic processor is designed which adopt the different word length input data operate in parallel fashion by single instruction multiple data (SIMD instruction. [9]. For better accuracy this is the effective way for managing power gated sleep signal generation dynamically compared to static method[10].

II. RELATED WORK

Xiaoxiao Zhang, et.al [1], This paper demonstrate 32× 32bit Multiprecision multiplier which results in reduction in power and circuit area as compare to conventational fixed width multiplier. This system is demonstrated with run-time workload adaptation. Performance of this system is good because it operates at the minimum supply voltage level and minimum clock frequency while meeting throughput requirements.

Manish Bhardwaj, et.al [2], This paper, defines how the power awareness can be enhanced using a *systematic* technique. Hierarchy of VLSI systems are made up from—multipliers, register files, digital filters, dynamic voltage-scaled processors, and data-gathering wireless networks at several levels. It is seen that, as a result, the power awareness of these preceding systems can be significantly enhanced leading to increases in battery lifetime.

Alice Wang, et.al [3], Scalability is needed for system if the environment of the device changes constantly. This paper focuses on design which qualifies the Energy-aware design with scale down energy as main feature. A new energy-scalable 8 and 16-bit precision support systems design proposed for a Real-valued FFT.

Kwen-Siong Chong, et.al [4], The new multiplier architecture is designed with features very low power and reduced spurious switching. The proposed micropower multiplier reduces switching activity by adding latch in adder block to use latches to synchronize the inputs to the adders in the Adder Block in a predetermined chronological sequence.

Magnus Sjalander, et. al [5], this states that the in recently the reconfigurable functional block uses in embedded system development because they having capacity to dynamically adapt the computational requirements of applications. The twin-precision (TP) multiplier [1] can switch between *N*-bit and *N*/2-bit precision multiplications without significant performance and area overhead.

S.-R. Kuang, et.al [6], The effective dynamic range of input operand is limited in multiplier due to that output is rounded off of truncated to limit the word size. Low-power signed pipelined truncated multiplier is proposed that can dynamically detect multiple combinations of input ranges and deactivate a large amount of unwanted transitions to reduce power consumption.

III. PROPOSED METHOD

The objective of this project is to implement an Input oriented dynamic scaling for multiplier on FPGA (spartan3) with low voltage supply and clock frequency.

- To implement system which uses the low voltage required silicon area, with output at different precision level.
- To achieve the power optimization at architecture level this system is designed and which is offering good performance at low supply voltage and frequency.
- To avoid unnecessary use of voltage supply from Vdd to ground voltage and frequency scaling is done.
- To disable the unused section of silicon area range detection is carried out with scanning of input.
- To Address the issues of fix length ASIC's.

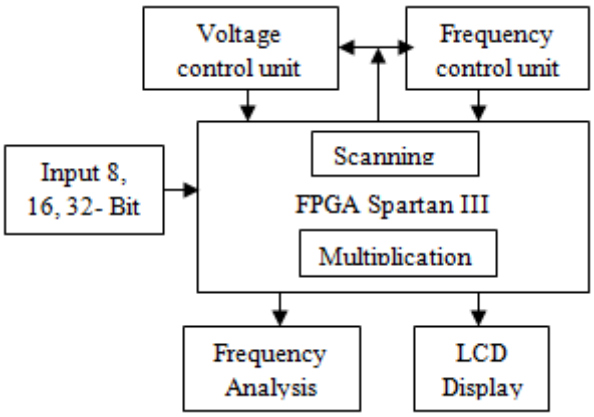


Fig. 1: Architecture of multiplier system

Basically the contribution of the proposed work is power optimization at architecture level. There are different power optimization techniques at different level, i.e at process device level, circuit level, algorithmic level and system level. All these level can be modified at manufacturing level except the architectural level this paper is on architecture level i.e. voltage scaling and frequency scaling. Power awareness, low cost , small silicon die , efficiency are important factor of VLSI system. All applications are tested before development board, or in software Xilinx, Cadence. VLSI chips are used in all branches of Engineering.

Area no of transistors in chip and supply voltage of such chips should be according to requirement to application is main aim of this system. In this paper the dynamic system is designed for multiplier with Frequency and voltage Scaling technique which works according to runtime workload given to system at different precision level.

IV. METHODOLOGY

Basically system divides in major three scenarios these are scanning for range detection of input data, DVFS and Multiplier which works on different power rails and frequency and multiplication of 8,16,32-Bit data at different voltage rage i.e. 3.3V to 1.25 V and frequency is 32MHz to 8MHz respectively.

A. Input to the system

Input to the system 8, 16, 32-Bit, 8-bit input is given to system through dip switches, and 16, 32 Bit input is given through software. In the multiplication m1, m2, I.e. multiplier, and multiplicand are needed in 8bit we can give it through hardware general input output pins are available but in 16 and 32Bit case this is not possible because it requires 32, 64 input pins so, this is given through software.

B. Scanning to detect the range Input

As the input data is not fixed at every time it changes according to requirement of applications so, that input data should be scanned. Scanning is important and first step in range detection. Control signals are generated from scanning 1, 2, 3 for 8, 16, 32,-bit according to input data that control signals are given to voltage and frequency scaling unit. If the inputs are lower than or equal to 128 i.e. data is of 8bit then control signal will be 1, inputs are lower than or equal to 32768 i.e. data is of 16bit then control signal will be 2, inputs are lower than or equal to 2147483648 i.e. data is of 32bit then control signal will be 32. According to that control signals voltage and frequency is scaled down and provided to multiplier for further process. From that only the required hardware is used, and unused sections should be disabled by providing only required voltage supply and frequency.

C. Voltage Scaling

Voltage scaling is done to reduce the power consumption. There is static and dynamic power in the circuit , dynamic power can be reduced by reducing voltage and clock frequency because we knows dynamic power is directly proportional to square of voltage and frequency to it. Here the dynamically power is reduced by reducing the voltage and frequency for the operation with proving according to requirement of input to system due to this the power in the circuit is less as compare to traditional method because in the traditional method voltage supply is fixed and independent on input. Voltage for 8,16,32bit is 1.25V, 2.5V, 3.3V respectively.

D. frequency Scaling

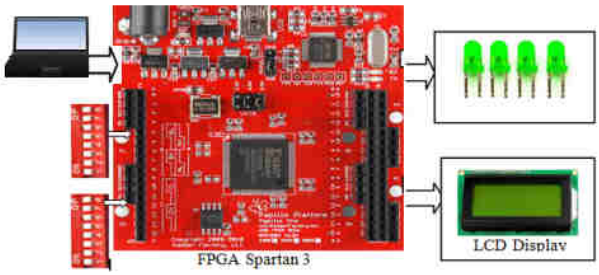
For the power conservation frequency scaling done. Dynamic frequency scaling is a technique in system architecture where by frequency of system can be automatically adjusted according to requirement. Voltage requirement for stable operation is determined by frequency at which circuit is clocked. Here the scaling is for 3 types of input data .Control signal can be 1, 2, and 3 decision will take place according is as follows .If control signal is 1 then scanned data is of 8-bit frequency scaled down to f_8=F/4 i.e. 8MHz, control signal is 2 then scanned data is of 16-bit frequency scaled down to f_{16}=F/2 i.e. 16MHz, control signal is 3 then scanned data is of 32-bit frequency is f_{32}=F i.e. 32MHz.

E. Multiplication

There are main 3 control signals which instructs the multipier for multiplication operation that are scanning voltage and frequency. Once the input range is scanned and detected the operating voltage and frequncy are tuned automatically. Operation can be perfomed on different data bit, 8×8, 8×16, 16×16, 8×32, 16×8, 16×32, 32×32, 32×16. The control signal are generated according to highest priority of input data. In the traditional system delays and spurious signal generation is more due to the cascsde chain of adder is used this is overcome with the use of koggstone adder .

V. EXPERIMENTAL SETUP AND RESULTS

FPGA Spartan 3E is used for implementation of dynamic system in terms of voltage and frequency.



LCD Display Input is detected and frequency, voltage range scaled and results displays on LCD. ***Frequency Analysis***4-LEDs are implemented for effectively analyzing frequency scaling on hardware. As scaled frequency for 8-bit is 8MHz, counter blinking rate is slower than at 16 MHz or 32MHz. LED blinking is totally depends on the magnitude of frequency. Voltage scaled output is display by LCD.

VI. RESULTS

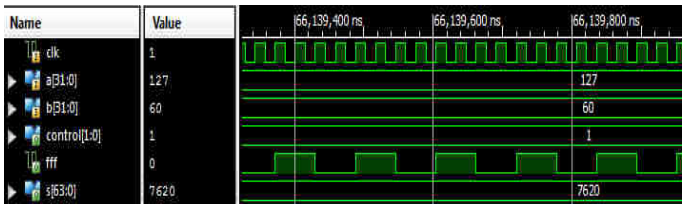


Fig.2: Simulation result of multiplication for 8-bit data

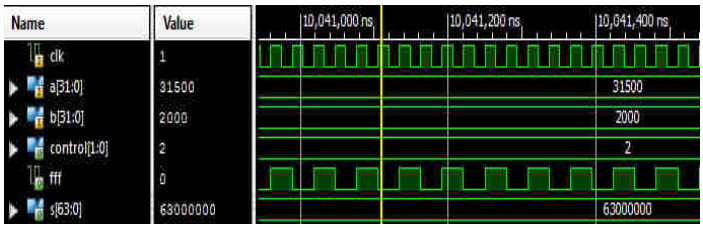


Fig.3: Simulation result of multiplication for16-bit data

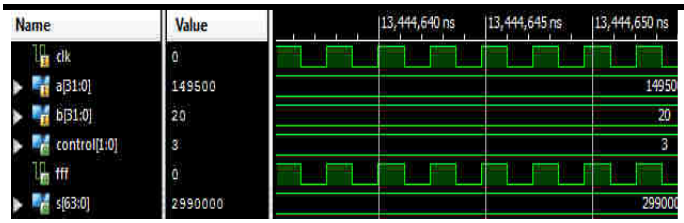


Fig.4: Simulation result of meeultiplication for32-bit data

Fig.5: Multiplication result for 8-bit data by LCD.

Fig.6: Multiplication result for 8-bit data by LCD.

Fig.7. Multiplication result for 8-bit data by LCD.

VII. CONCLUSION

The input oriented dynamic voltage and frequency scaling is done on FPGA at low supply voltage and frequency. Power optimization is achieved at architecture level. According to requirement of input the gates are used and disabled unused section so silicon area is effectively used .The effective adder used in this circuit by that switching of spurious signal reduced.

ACKNOWLEDGEMENTS

The accomplishment of this work is not only due to our efforts. In fact so, with great pleasure we take this opportunity to express our gratitude towards all the individuals who have helped and inspired us in this work.

REFERENCES

[1] X. Zhang, *Farid*and A.Bermak, "32 Bit×32 Bit Multiprecision Razor-Based Dynamic Voltage Scaling Multiplier With Operands Scheduler"*IEEE Trans on very large scale integration (vlsi) system*, vol.22, no.4, april 2014.

[2] M. Bhardwaj, R. Min, and A. Chandrakasan, "Quantifying and enhancing power awareness of VLSI systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 9, no. 6, pp. 757–772, Dec. 2001.

[3] A. Wang and A. Chandrakasan, "Energy-aware architectures for a realvalued FFT implementation," in *Proc. IEEE Int. Symp. Low Power Electron. Design*, Aug. 2003, pp. 360–365.

[4] K.-S. Chong, B.-H. Gwee, and J. S. Chang, "A micropower low-voltage multiplier with reduced spurious switching," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 2, pp. 255–265, Feb. 2005.

[5] M. Sjalander, M. Drazdziulis, P. Larsson-Edefors, and H. Eriksson,"A low-leakage twin-precision multiplier using reconfigurable power gating," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 1654–1657.

[6] S.-R. Kuang and J.-P. Wang, "Design of power-efficient pipelined truncated multipliers with various output precision," *IET Comput. Digital Tech.*, vol. 1, no. 2, pp. 129–136, Mar. 2007.

[7] J. L. Holt and J.-N. Hwang, "Finite precision error analysis of neural network hardware implementations," IEEE Trans. Comput., vol. 42, no. 3, pp. 281–290, Mar. 1993.

[8] A. Bermak, D. Martinez, and J.-L. Noullet, "High-density 16/8/4-bit configurable multiplier," Proc. Inst. Electr. Eng. Circuits Devices Syst., vol. 144, no. 5, pp. 272–276, Oct. 1997.

[9] S. Perri, P. Corsonello, M. A. Iachino, M. Lanuzza, and G. Cocorullo, "Variable precision arithmetic circuits for FPGA-based multimedia processors," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 9, pp. 995–999, Sep. 2004.

[10] A. Youssef, M. Anis, and M. Elmasry, "A comparative study between static and dynamic sleep signal generation techniques for leakage tolerant designs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 9, pp. 1114–1126, Sep. 2008.